

# TQC2025B

## AEC-Q100, High Frequency, Single-Chip, One-Output Clock Generator

TOKYO QUARTZ CO.,LTD

### Features

- AEC-Q100 with extended temperature range (-55°C to 125°C)
- Frequencies between 115.2 MHz and 137 MHz accurate to 6 decimal points
- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as  $\pm 20$  ppm
- Industry best G-sensitivity of 0.1 PPB/G
- LVCMOS/LVTTL compatible output
- 5-pin SOT23-5 package: 2.9 x 2.8 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

### Applications

- Automotive, extreme temperature and other high-rel electronics
- Infotainment systems, collision detection devices, and in-vehicle networking
- Power train control



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### Electrical Specifications

**Table 1. Electrical Characteristics**

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
Output Frequency Range	f	115.20	–	137	MHz	Refer to <a href="#">Table 14</a> and <a href="#">Table 15</a> for the exact list of supported frequencies
<b>Frequency Stability and Aging</b>						
Frequency Stability	F <sub>stab</sub>	-20	–	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF $\pm$ 10%).
		-25	–	+25	ppm	
		-30	–	+30	ppm	
		-50	–	+50	ppm	
<b>Operating Temperature Range</b>						
Operating Temperature Range (ambient)	T <sub>use</sub>	-40	–	+85	°C	Industrial, AEC-Q100 Grade 3
		-40	–	+105	°C	Extended Industrial, AEC-Q100 Grade 2
		-40	–	+125	°C	Automotive, AEC-Q100 Grade 1
		-55	–	+125	°C	Extended Temperature, AEC-Q100
<b>Supply Voltage and Current Consumption</b>						
Supply Voltage	V <sub>dd</sub>	1.62	1.8	1.98	V	All voltages between 2.25V and 3.63V including 2.5V, 2.8V, 3.0V and 3.3V are supported. Contact <a href="#">TQC</a> for 1.5V support
		2.25	–	3.63	V	
Current Consumption	I <sub>dd</sub>	–	6	8	mA	No load condition, f = 125 MHz, V <sub>dd</sub> = 2.25V to 3.63V
		–	4.9	6	mA	No load condition, f = 125 MHz, V <sub>dd</sub> = 1.62V to 1.98V
<b>LVCMOS Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	1.5	3	ns	V <sub>dd</sub> = 2.25V - 3.63V, 20% - 80%
		–	1.5	2.5	ns	V <sub>dd</sub> = 1.8V, 20% - 80%
Output High Voltage	VOH	90%	–	–	V <sub>dd</sub>	IOH = -4 mA (V <sub>dd</sub> = 3.0V or 3.3V) IOH = -3 mA (V <sub>dd</sub> = 2.8V and V <sub>dd</sub> = 2.5V) IOH = -2 mA (V <sub>dd</sub> = 1.8V)
Output Low Voltage	VOL	–	–	10%	V <sub>dd</sub>	IOL = 4 mA (V <sub>dd</sub> = 3.0V or 3.3V) IOL = 3 mA (V <sub>dd</sub> = 2.8V and V <sub>dd</sub> = 2.5V) IOL = 2 mA (V <sub>dd</sub> = 1.8V)
<b>Input Characteristics</b>						
Input High Voltage	VIH	70%	–	–	V <sub>dd</sub>	Pin 1, OE
Input Low Voltage	VIL	–	–	30%	V <sub>dd</sub>	Pin 1, OE
Input Pull-up Impedance	Z <sub>in</sub>	–	100	–	k $\Omega$	Pin 1, OE logic high or logic low
<b>Startup and Resume Timing</b>						
Startup Time	T <sub>start</sub>	–	–	5	ms	Measured from the time V <sub>dd</sub> reaches its rated minimum value
Enable/Disable Time	T <sub>oe</sub>	–	–	130	ns	f = 115.20 MHz. For other frequencies, T <sub>oe</sub> = 100 ns + 3 * cycles
<b>Jitter</b>						
RMS Period Jitter	T <sub>jitt</sub>	–	1.6	2.5	ps	f = 125 MHz, 2.25V to 3.63V
		–	1.8	3	ps	f = 125 MHz, 1.8V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.7	–	ps	f = 125 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.5	–	ps	f = 125 MHz, Integration bandwidth = 12 kHz to 20 MHz

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## AEC-Q100, High Frequency, Single-Chip, One-Output Clock Generator

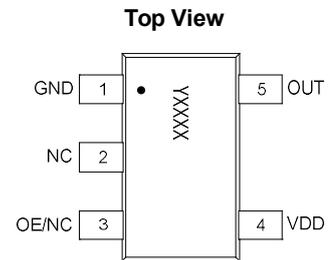
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**Table 2. Pin Description**

Pin	Symbol		Functionality
1	GND	Power	Electrical ground <sup>[1]</sup>
2	NC	No Connect	No connect
3	OE/NC	Output Enable	H <sup>[2]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled.
		No Connect	Any voltage between 0 and Vdd or Open <sup>[2]</sup> : Specified frequency output. Pin 3 has no function.
4	VDD	Power	Power supply voltage <sup>[1]</sup>
5	OUT	Output	Oscillator output

**Notes:**

1. A capacitor of value 0.1  $\mu$ F or higher between Vdd and GND is required.
2. In OE or ST mode, a pull-up resistor of 10 k $\Omega$  or less is recommended if pin 3 is not externally driven. If pin 3 needs to be left floating, use the NC option.



**Figure 1. Pin Assignments**

**Table 3. Absolute Maximum Limits**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	$^{\circ}$ C
Vdd	-0.5	4	V
Electrostatic Discharge	-	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	-	260	$^{\circ}$ C
Junction Temperature <sup>[3]</sup>	-	150	$^{\circ}$ C

**Note:**

3. Exceeding this temperature for extended period of time may damage the device.

**Table 4. Thermal Consideration<sup>[4]</sup>**

Package	$\theta$ JA, 4 Layer Board ( $^{\circ}$ C/W)	$\theta$ JC, Bottom ( $^{\circ}$ C/W)
SOT23-5	421	175

**Note:**

4. Refer to JESD51 for  $\theta$ JA and  $\theta$ JC definitions, and reference layout used to determine the  $\theta$ JA and  $\theta$ JC values in the above table.

**Table 5. Maximum Operating Junction Temperature<sup>[5]</sup>**

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
85 $^{\circ}$ C	95 $^{\circ}$ C
105 $^{\circ}$ C	115 $^{\circ}$ C
125 $^{\circ}$ C	135 $^{\circ}$ C

**Note:**

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

**Table 6. Environmental Compliance**

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method2003
Moisture SenTQCivity Level	MSL1 @ 260 $^{\circ}$ C

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### Test Circuit and Waveform<sup>[6]</sup>

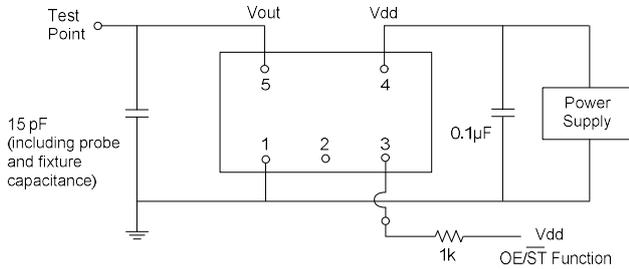


Figure 2. Test Circuit

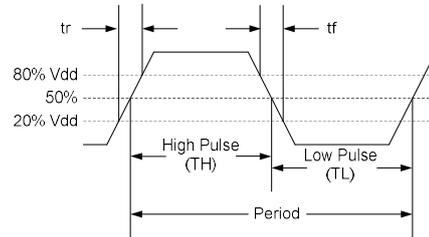


Figure 3. Waveform

**Note:**

6. TQC2025 has “no runt” pulses and “no glitch” output during startup or resume.

### Timing Diagrams

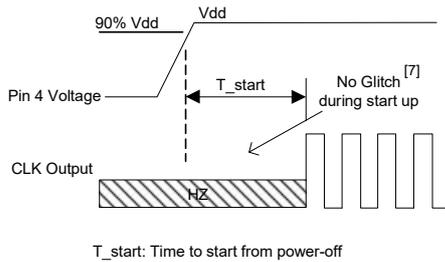


Figure 4. Startup Timing (OE Mode)

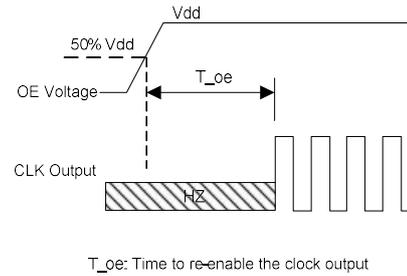


Figure 5. OE Enable Timing (OE Mode Only)

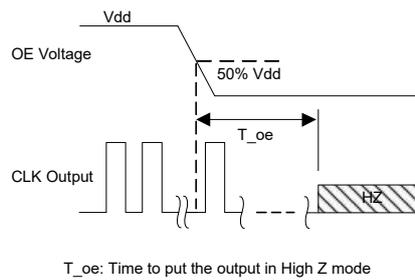


Figure 6. OE Disable Timing (OE Mode Only)

**Note:**

7. TQC2025 has “no runt” pulses and “no glitch” output during startup or resume.

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## Performance Plots<sup>[8]</sup>

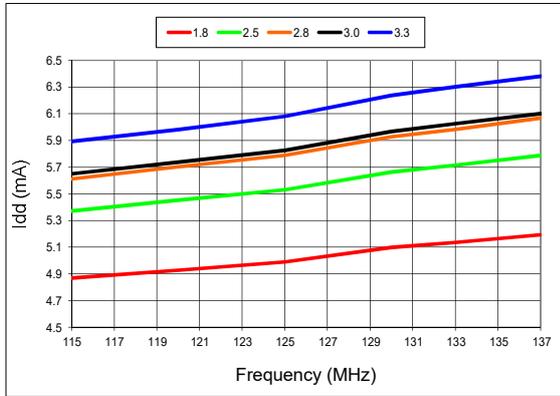


Figure 7. Idd vs Frequency

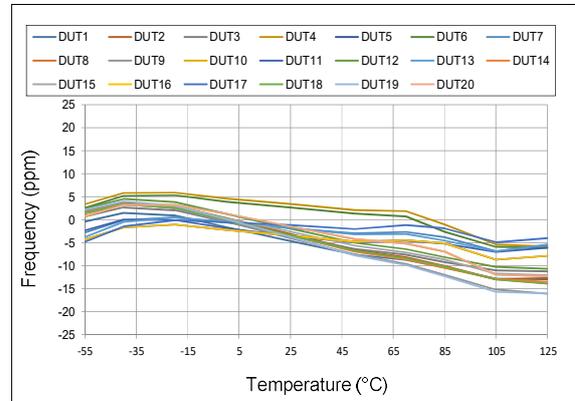


Figure 8. Frequency vs Temperature

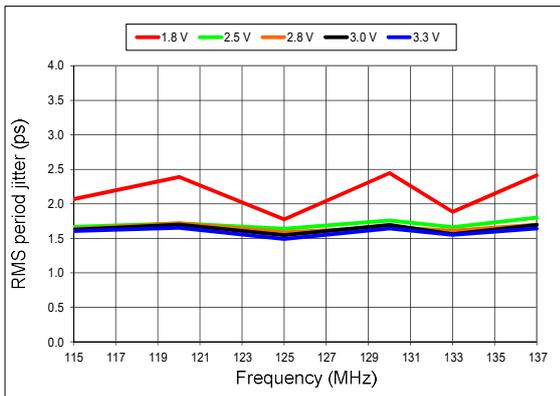


Figure 9. RMS Period Jitter vs Frequency

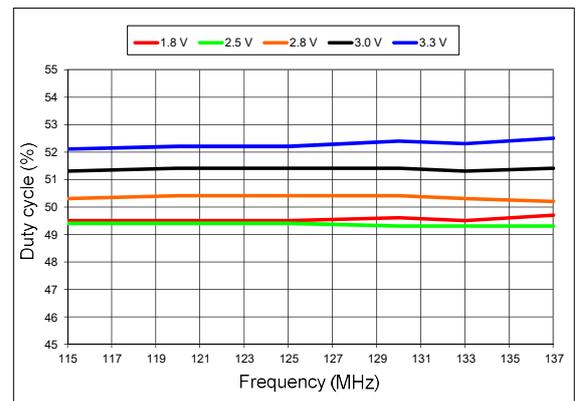


Figure 10. Duty Cycle vs Frequency

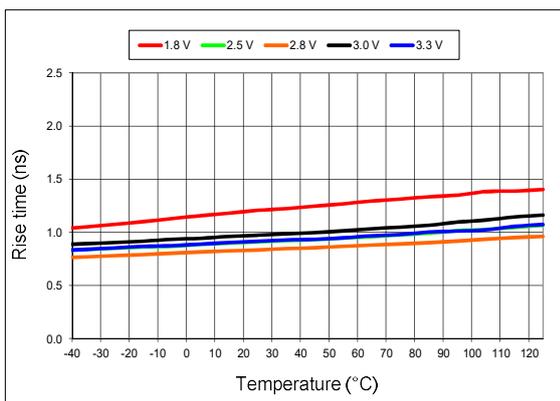


Figure 11. 20%-80% Rise Time vs Temperature

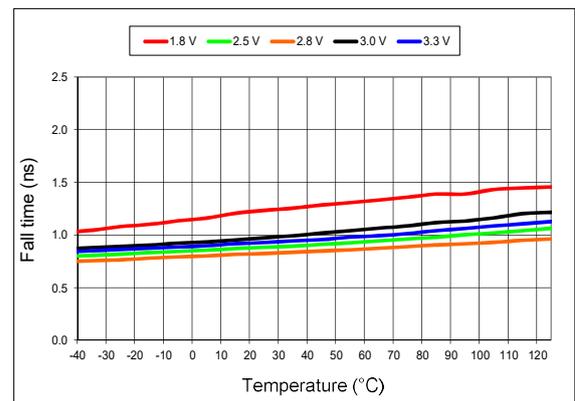


Figure 12. 20%-80% Fall Time vs Temperature

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## Performance Plots<sup>[8]</sup>

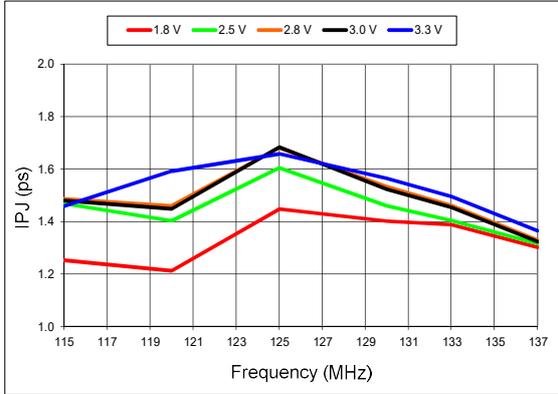


Figure 13. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency<sup>[9]</sup>

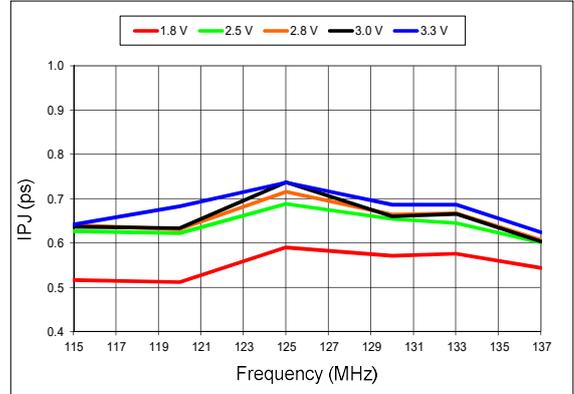


Figure 14. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency<sup>[9]</sup>

### Notes:

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
9. Phase noise plots are measured with Agilent E5052B signal source analyzer.

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### Programmable Drive Strength

The TQC2025 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the TQC Application Notes section:

### EMI Reduction by Slowing Rise/Fall Time

Figure 15 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

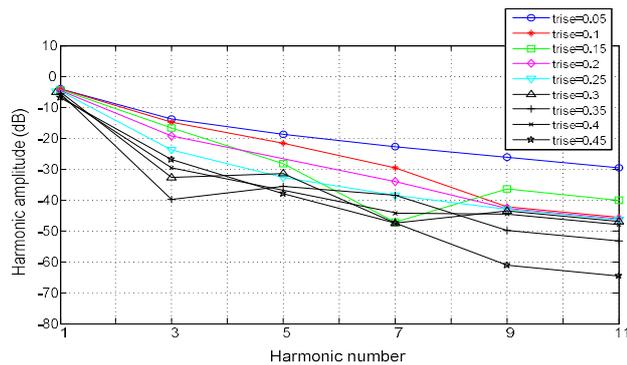


Figure 15. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

### Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

### High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V TQC2025 device with default drive strength setting, the typical rise/fall time is 0.46ns for 5 pF output load. The typical rise/fall time slows down to 1 ns when the output load increases to 15 pF. One can choose to speed up the rise/fall time to 0.72 ns by then increasing the driven strength setting on the TQC2025 to "F".

The TQC2025 can support up to 30 pF in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Fall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

### TQC2025 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the TQC2025 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf}_{20/80}}$$

where Trf<sub>20/80</sub> is the typical value for 20%-80% rise/fall time.

#### Example 1

Calculate f<sub>MAX</sub> for the following condition:

- V<sub>dd</sub> = 3.3V (Table 11)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.46 ns (rise/fall time part number code = U)

Part number for the above example:

TQC2025BAE12-18E-137.000000



Drive strength code is inserted here. Default setting is "-"

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## Rise/Fall Time (20% to 80%) vs C<sub>LOAD</sub> Tables

Table 7. V<sub>dd</sub> = 1.8V Rise/Fall Times for Specific C<sub>LOAD</sub>

Rise/Fall Time Typ (ns)		
Drive Strength \ C <sub>LOAD</sub>	5 pF	
T	0.93	n/a
E	0.78	n/a
U	0.70	1.48
F or "-": default	0.65	1.30

Table 8. V<sub>dd</sub> = 2.5V Rise/Fall Times for Specific C<sub>LOAD</sub>

Rise/Fall Time Typ (ns)		
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF
R	1.45	n/a
B	1.09	n/a
T or "-": default	0.62	1.28
E	0.54	1.00
U	0.43	0.96
F	0.34	0.88

Table 9. V<sub>dd</sub> = 2.8V Rise/Fall Times for Specific C<sub>LOAD</sub>

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T or "-": default	0.55	1.12	n/a
E	0.44	1.00	n/a
U	0.34	0.88	n/a
F	0.29	0.81	1.48

Table 10. V<sub>dd</sub> = 3.0V Rise/Fall Times for Specific C<sub>LOAD</sub>

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.22	n/a	n/a
B	0.89	n/a	n/a
T or "-": default	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

Table 11. V<sub>dd</sub> = 3.3V Rise/Fall Times for Specific C<sub>LOAD</sub>

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.16	n/a	n/a
B	0.81	n/a	n/a
T or "-": default	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

**Note:**

10. "n/a" indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available.

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### Pin 1 Configuration Options (OE or NC)

Pin 1 of the TQC2025 can be factory-programmed to support two modes: Output Enable (OE) or No Connect (NC). These modes can also be programmed with the Time Machine using field programmable devices.

#### Output Enable (OE) Mode

In the OE mode, applying logic low to the OE pin only disables the output driver and putTQC in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in  $<1\mu\text{s}$ .

#### No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE or NC mode.

Table 12. OE vs. NC

	OE	NC
Active current 125 MHz (max, 1.8V)	6 mA	6 mA
OE disable current (max, 1.8V)	4 mA	N/A
OE enable time at 110 MHz (max)	130 ns	N/A
Output driver in OE disable	High Z	N/A

#### Output on Startup and Resume

The TQC2025 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup.

In addition, the TQC2025 supports “no runt” pulses and “no glitch” output during startup or when the output driver is re-enabled from the OE disable mode as shown in the waveform captures in Figure 16 and Figure 17.



Figure 16. Startup Waveform vs. Vdd

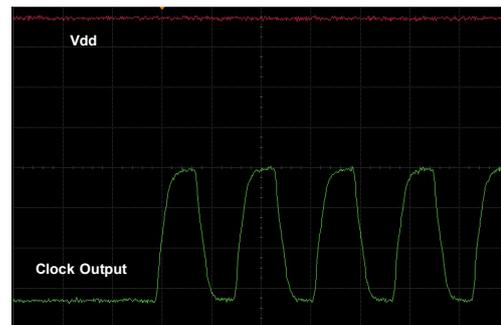


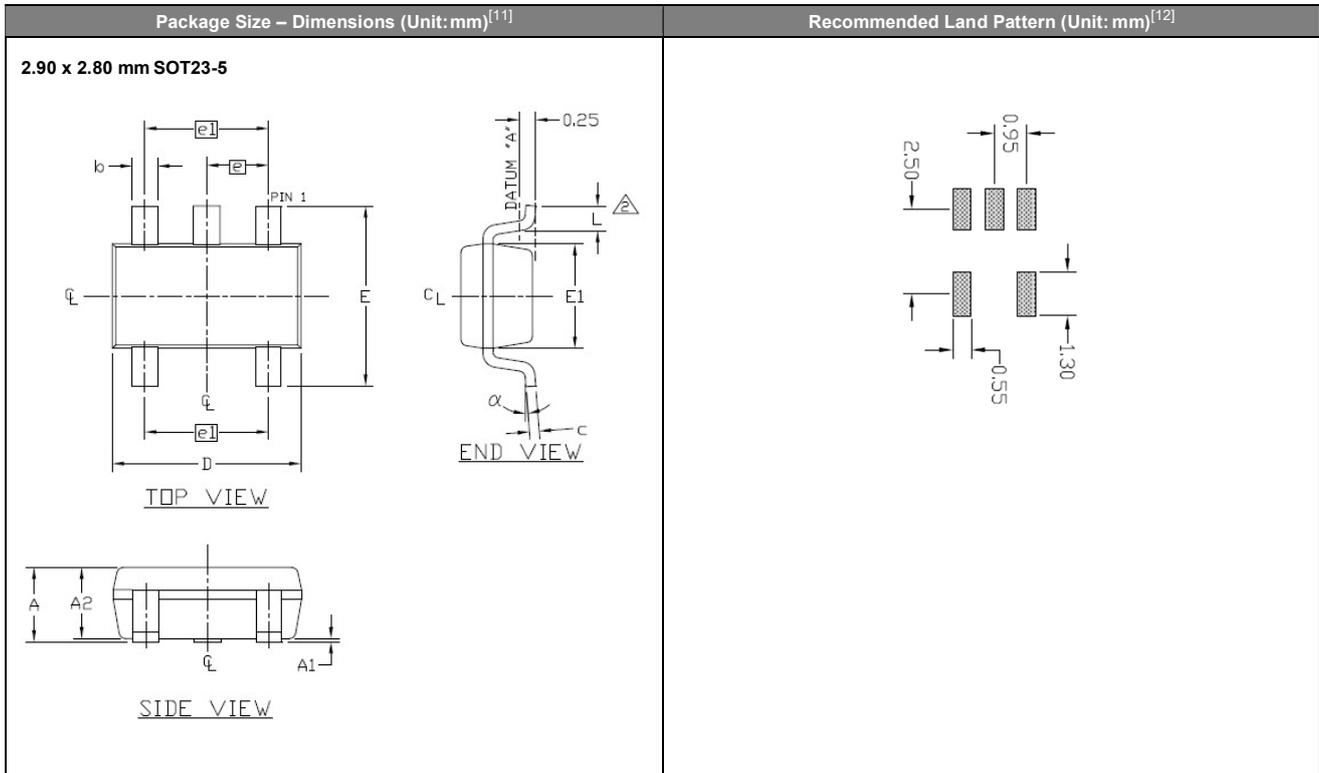
Figure 17. Startup Waveform vs. Vdd  
(Zoomed-in View of Figure 16)

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## Dimensions and Patterns



**Notes:**

- 11. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- 12. A capacitor value of 0.1  $\mu$ F between Vdd and GND is required.

**Table 13. Dimension Table**

Symbol	Min.	Nom.	Max.
A	0.90	1.27	1.45
A1	0.00	0.07	0.15
A2	0.90	1.20	1.30
b	0.30	0.35	0.50
c	0.14	0.15	0.20
D	2.75	2.90	3.05
E	2.60	2.80	3.00
E1	1.45	1.60	1.75
L	0.30	0.38	0.55
L1	0.25 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
$\alpha$	0°	–	8°

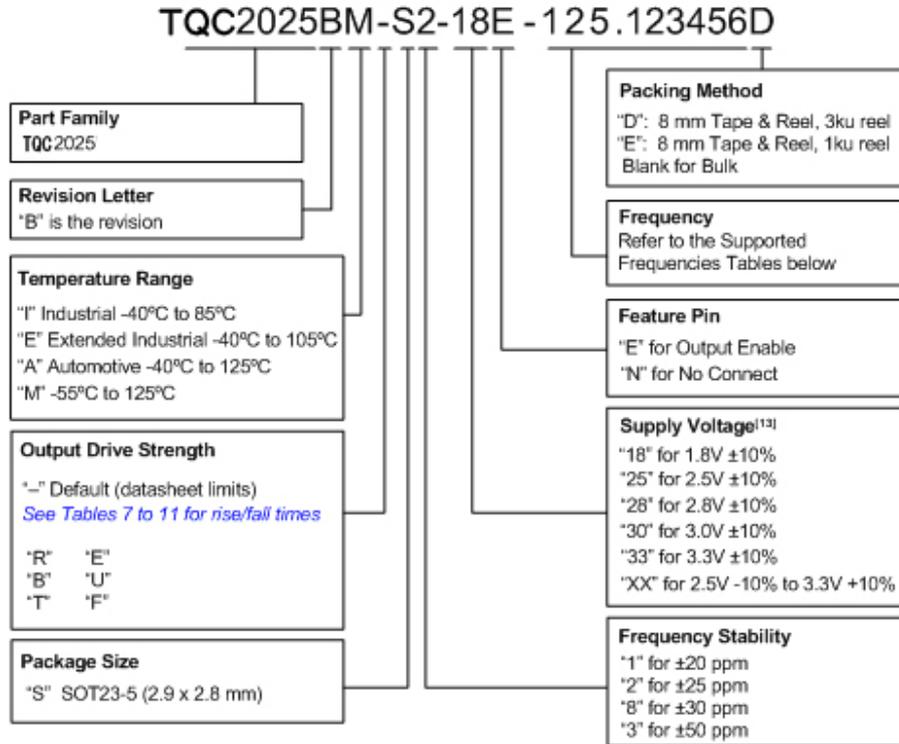
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## Ordering Information

The Part No. Guide is for reference only. To customize and build an exact part number, use the TQC [Part Number Generator](#).



**Note:**

13. The voltage portion of the TQC2025 part number consists of two characters that denote the specific supply voltage of the device. The TQC2025 supports either 1.8V ±10% or any voltage between 2.25V and 3.62V. In the 1.8V mode, one can simply insert 18 in the part number. In the 2.5V to 3.3V mode, two digits such as 18, 25 or 33 can be used in the part number to reflect the desired voltage. Alternatively, "XX" can be used to indicate the entire operating voltage range from 2.25V to 3.63V.

**Table 14. Supported Frequencies (-40°C to +85°C)<sup>[14]</sup>**

Frequency Range	
Min.	Max.
115.200000 MHz	137.000000 MHz

**Table 15. Supported Frequencies (-40°C to +105°C or -40°C to +125°C)<sup>[14, 15]</sup>**

Frequency Range	
Min.	Max.
115.194001 MHz	117.810999 MHz
118.038001 MHz	118.593999 MHz
118.743001 MHz	122.141999 MHz
122.705001 MHz	123.021999 MHz
123.348001 MHz	137.000000 MHz

**Table 16. Supported Frequencies (-55°C to +125°C)<sup>[14, 15]</sup>**

Frequency Range	
Min.	Max.
119.342001 MHz	120.238999 MHz
120.262001 MHz	121.169999 MHz
121.243001 MHz	121.600999 MHz
123.948001 MHz	137.000000 MHz

**Notes:**

- 14. Any frequency within the min and max values in the above table are supported with 6 decimal places of accuracy.
- 15. Please contact TQC for frequencies that are not listed in the tables above.

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## AEC-Q100, High Frequency, Single-Chip, One-Output Clock Generator

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Table 17. Additional Information

Document	Description	Download Link
Time Machine II	MEMS oscillator programmer	
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	
Qualification Reports	RoHS report, reliability reports, compoTQCion	
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	
Termination Techniques	Termination design recommendations	
Layout Techniques	Layout recommendations	

## Revision History

Table 18. Datasheet Version and Change Log

Revision	Release Date	Change Summary
1.0	5/28/15	Final production release
1.1	3/18/15	Added support for $\pm 20$ ppm frequency stability Revised the dimension table Added the industrial temperature “-40°C to $\pm 85^\circ\text{C}$ ” option

# TQC2025B

## AEC-Q100, High Frequency, Single-Chip, One-Output Clock Generator

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### Silicon MEMS Outperforms Quartz

#### Best Reliability

Silicon is inherently more reliable than quartz. Figure 1 shows a comparison with quartz technology.

#### Why is EpiSeal™ MEMS Best in Class:

- EpiSeal MEMS resonators are hermetically vacuum-sealed during wafer processing, which eliminates foreign particles and improves long term aging and reliability
- MEMS resonator is paired with advanced analog IC

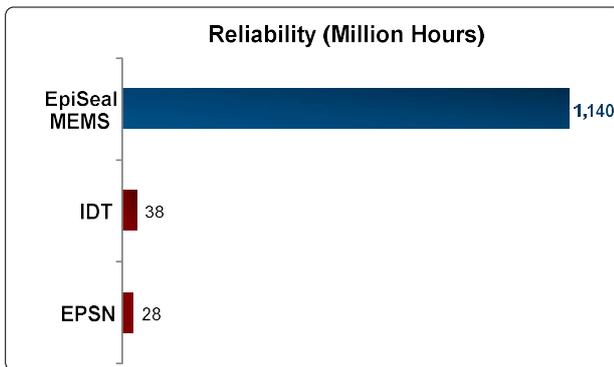


Figure 1. Reliability Comparison<sup>[1]</sup>

#### Best Aging

Unlike quartz, EpiSeal MEMS oscillators have excellent long-term aging performance which is why every new EpiSeal MEMS product specifies 10-year aging.

#### Why is EpiSeal MEMS Best in Class:

- EpiSeal MEMS resonators are hermetically vacuum-sealed during wafer processing, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

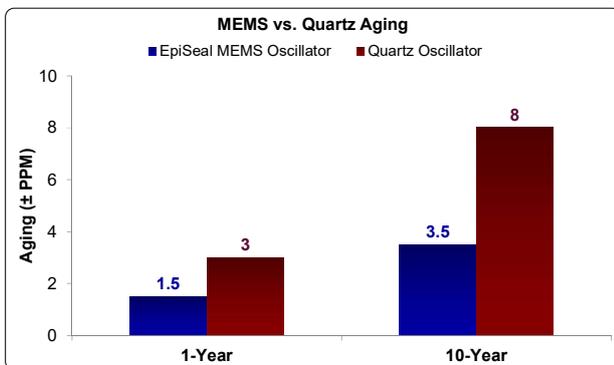


Figure 2. Aging Comparison<sup>[2]</sup>

#### Best Electro Magnetic Susceptibility (EMS)

EpiSeal MEMS oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

#### Why is EpiSeal MEMS Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

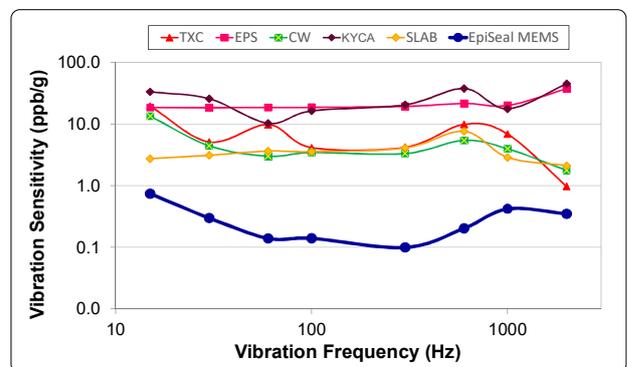


Figure 3. Electro Magnetic Susceptibility (EMS)<sup>[3]</sup>

#### Best Power Supply Noise Rejection

EpiSeal MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

#### Why is EpiSeal MEMS Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- MEMS resonator is paired with advanced analog CMOS IC

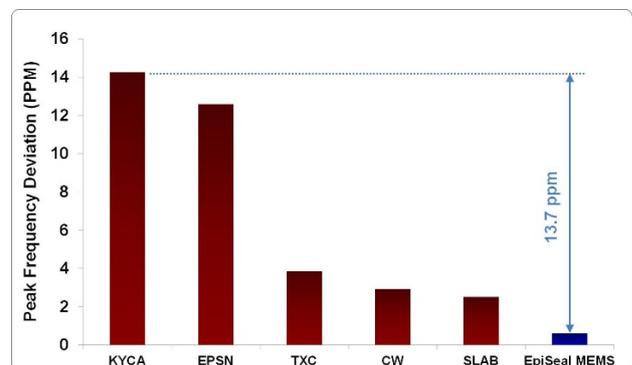


Figure 4. Power Supply Noise Rejection<sup>[4]</sup>

# TQC2025B

## AEC-Q100, High Frequency, Single-Chip, One-Output Clock Generator

TOKYO QUARTZ CO.,LTD

### Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

#### Why is EpiSeal MEMS Best in Class:

- The moving mass of MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

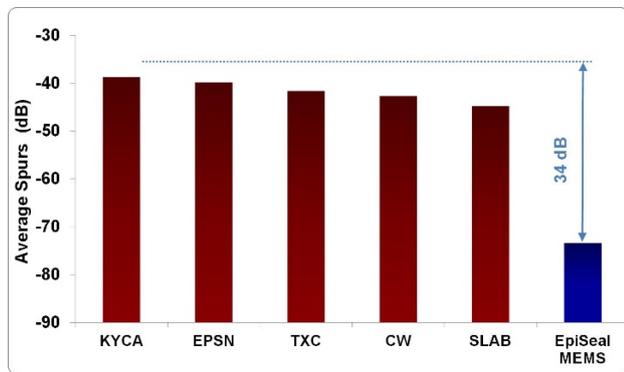


Figure 5. Vibration Robustness<sup>[5]</sup>

### Best Shock Robustness

EpiSeal MEMS oscillators can withstand at least 50,000g shock. They maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

#### Why is EpiSeal MEMS Best in Class:

- The moving mass of MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

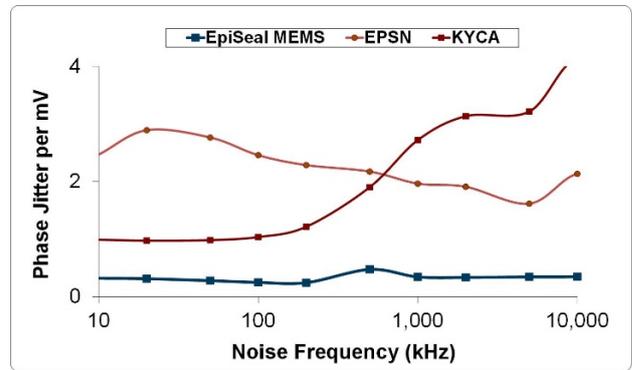


Figure 6. Shock Robustness<sup>[6]</sup>

#### Figure labels:

- TXC = TXC
- Epson = EPSN
- Connor Winfield = CW
- Kyocera = KYCA
- SiLabs = SLAB
- TQC = EpiSeal MEMS

# TQC2025B

## AEC-Q100, High Frequency, Single-Chip, One-Output Clock Generator

TOKYO QUARTZ CO.,LTD

### Notes:

1. Data source: Reliability documents of named companies.
2. Data source: TQCime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
  - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
  - Field strength: 3V/m
  - Radiated signal modulation: AM 1 kHz at 80% depth
  - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
  - Antenna polarization: Vertical
  - DUT position: Center aligned to antenna

#### Devices used in this test:

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	TQC	TQC9120AC-1D2-33E156.250000	MEMS + PLL
EPSN	Epson	EG-2102CA156.2500M-PHPAL3	Quartz, SAW
TXC	TXC	BB-156.250MBE-T	Quartz, 3 <sup>rd</sup> Overtone
CW	Conner Winfield	P123-156.25M	Quartz, 3 <sup>rd</sup> Overtone
KYCA	AVX Kyocera	KC7050T156.250P30E00	Quartz, SAW
SLAB	SiLab	590AB-BDG	Quartz, 3 <sup>rd</sup> Overtone + PLL

4. 50 mV pk-pk Sinusoidal voltage.

#### Devices used in this test:

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	TQC	TQC8208AI-33-33E-25.000000	MEMS + PLL
NDK	NDK	NZ2523SB-25.6M	Quartz
KYCA	AVX Kyocera	KC2016B25M0C1GE00	Quartz
EPSN	Epson	SG-310SCF-25M0-MB3	Quartz

#### 5. Devices used in this test:

same as EMS test stated in Note 3.

#### 6. Test conditions for shock test:

- MIL-STD-883F Method 2002
- Condition A: half sine wave shock pulse, 500-g, 1ms
- Continuous frequency measurement in 100  $\mu$ s gate time for 10 seconds

#### Devices used in this test:

same as EMS test stated in Note 3.

7. Additional data, including setup and detailed results, is available upon request to qualified customer.