TQC1566 Preliminary

1.2mm^2 Micropower, 5 ppm, Low-Jitter 32.768 kHz Super TCXO

TOKYO QUARTZ CO.,LTD

Features

- 32.768 kHz ±5 ppm all-inclusive frequency stability
- World's smallest TCXO Footprint: 1.2 mm^2
  - 1.5 x 0.8 mm CSP
  - No external bypass cap required
- Improved stability reduces system power with fewer network timekeeping updates
- Ultra-low power: 4.5 µA
- Supply voltage: 1.8V ±10%
- Operating temperature ranges: -20°C to +70°C, -40°C to +85°C
- Pb-free, RoHS and REACH compliant

Applications

- Smart watches, health and wellness monitors
- Ultra-accurate RTC reference clock
- Smart utility meters, E-meters
- Internet-of-Things (IoT) with BLE

Note:
For overmolded applications that require the most accurate frequency, consider the TQC1568 super-TCXO with in-system auto-calibration.

Electrical Characteristics

Conditions: Min/Max limits are over temperature, Vdd = 1.8V ±10%, unless otherwise stated. Typicals are at 25°C and Vdd = 1.8V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Total Frequency Stability [1]	F_stab	-5		5	ppm	All inclusive, **without** overmold.
Allan Deviation	AD		1e-8	4e-8		1 second averaging time
First Year Frequency Aging	F_aging		±1		ppm	T_A = 25°C, Vdd = 1.8V
Jitter and Frequency Response Performance						
Integrated Phase Jitter	IPJ		1.8	2.5	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peaks inusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz.
RMS Period Jitter	PJ_{RMS}		2.5	4	ns_{RMS}	10,000 samples, per JEDEC standard 65B
Peak-to-Peak Period Jitter	PJ_{p-p}		20	35	ns_{p-p}	
Dynamic Temperature Frequency Response		-0.5		+0.5	ppm/sec	Under temp ramp up to 1.5°C/sec
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.62	1.8	1.98	V	
Supply Current	Idd		4.5	5.3	µA	No load
Start-up Time at Power-up	t_start			300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse.
Operating Temperature Range						
Operating Temperature Range	Op_Temp	-20		70	°C	"C" ordering code
		-40		85	°C	"I" ordering code
LVCMOS Output						
Output Rise/Fall Time	tr, tf		9	20	ns	
Output Clock Duty Cycle	DC	45		55	%	
Output Voltage High	VOH	90%			Vdd	I_{OH} = -1 µA
Output Voltage Low	VOL			10%	Vdd	I_{OL} = 1 µA

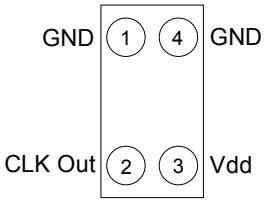
Note:

1. Relative to 32.768 kHz, includes initial tolerance, over temp stability, Vdd, 20% load variation, hysteresis, board-level underfill, 3x reflow. Tested with Agilent 53132A frequency counter. Measured with 100 ms gate time for accurate frequency measurement.

Pin Configuration

CSP Pin	Symbol	I/O	Functionality
1	GND	Internal Test	Connect to GND
2	CLK Out	OUT	Oscillator clock output.
3	Vdd	Power Supply	Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). TQC1566 includes on-chip filtering capacitors. Under extreme noise on the supply, a 10-100 nF low ESR ceramic bypass capacitor may be recommended close to the Vdd pin.
4	GND	Power Supply Ground	Connect to ground.

CSP Package (Top View)



Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4.0	V
Continuous Maximum Operating Temperature Range		105	°C
Short Duration Maximum Operating Temperature Range	≤ 30 minutes	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	20,000	*g*
Mechanical Vibration Resistance	Mil 883, Method 2007	70	*g*
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C

System Block Diagram

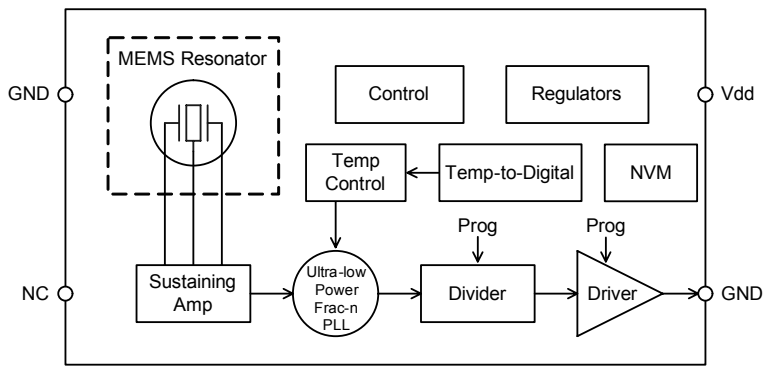


Figure 1. TQC1566 Block Diagram

Description

TQC1566 is an ultra-small, micropower 32.768 kHz TCXO optimized for battery-powered applications. TQC's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical supply current is 4.5 µA under no load condition.

TQC's MEMS oscillator consists of a MEMS resonator and a programmable analog circuit. TQC1566 MEMS resonator is built with TQC's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, TQC's MEMS resonator die can be used like any other semiconductor die. One unique result of TQC's MEMS First and EpiSeal manufacturing processes is the capability to integrate TQC's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

TCXO Frequency Stability

TQC1566 is factory calibrated (trimmed) over multiple temper- ature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C2 temperature coefficient, the TQC1566 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range.

When measuring the output frequency of TQC1566 with a frequency counter, it is important to make sure the counter's gate time is ≥100 ms. Shorter gate times may lead to inaccurate measurements.

Dynamic Temperature Frequency Response

Dynamic Temperature Frequency Response is the rate of frequency change during temperature ramps. This is an important performance metric when the oscillator is mounted near a high power component (e.g. SoC or power management) that may rapidly change the temperature of surrounding components.

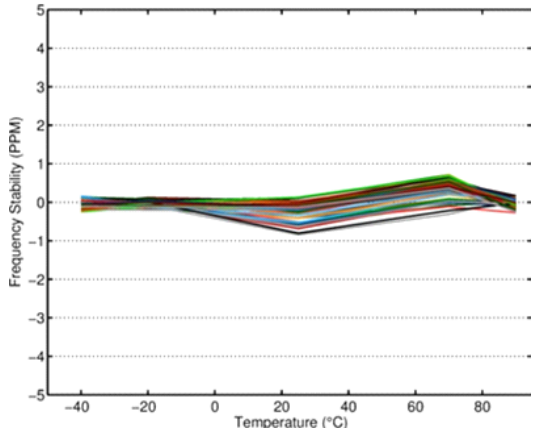
For moderate temperature ramp rates (< 2°C/sec), the dynamic response is primarily determined by the steady-state frequency vs. temperature of the device. The best dynamic response is obtained from parts which have been trimmed to be flat in frequency over temperature.

For high temperature ramp rates (>5°C/sec), the latency in the temperature compensation loop contributes a larger frequency error, which is dependent on the temperature compensation update rate. This part achieves excellent performance at 3Hz update rate. This device family supports faster update rates for further reducing dynamic frequency error at the expense of slightly increased current consumption.

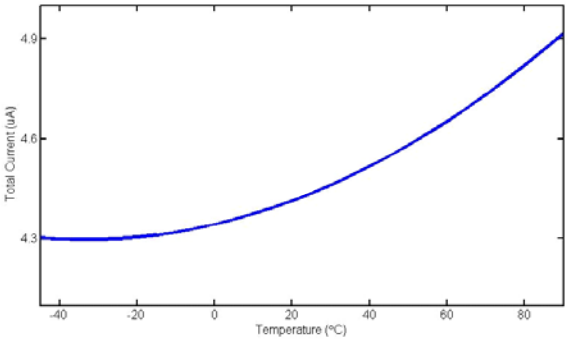
Typical Operating Curves

(T_A = 25°C, Vdd = 1.8V, unless otherwise stated)

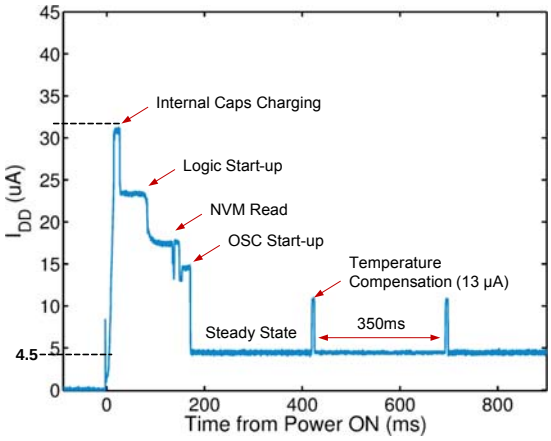
Frequency Stability over Temperature (Post Reflow)



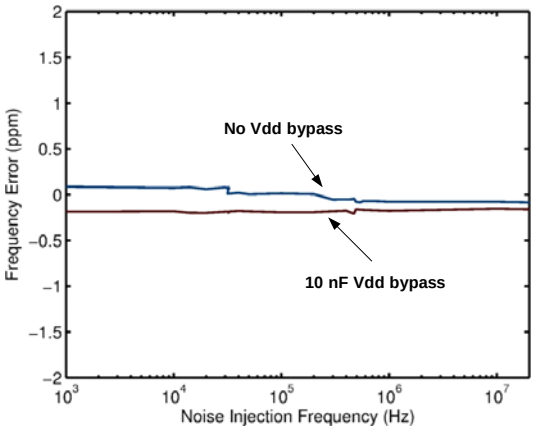
Supply Current over Temperature (No Load)



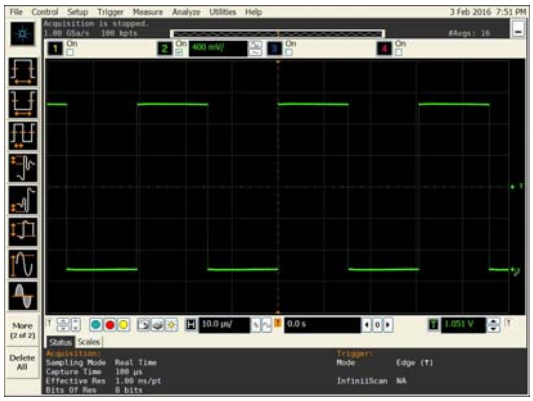
Start-up and Steady-State Current Profile



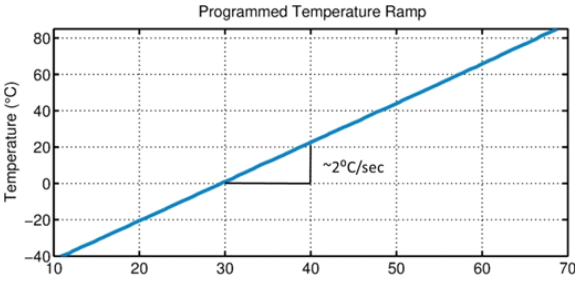
Power Supply Noise Rejection (PSNR)

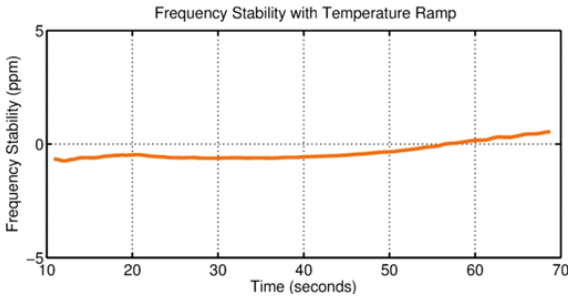


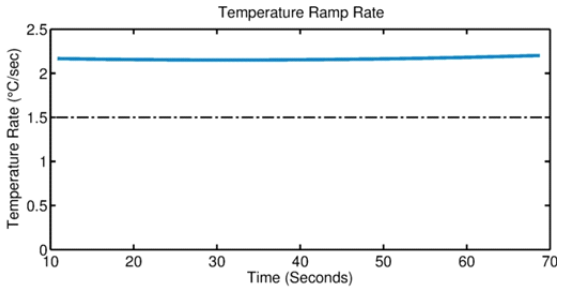
LVCMOS Output Swing

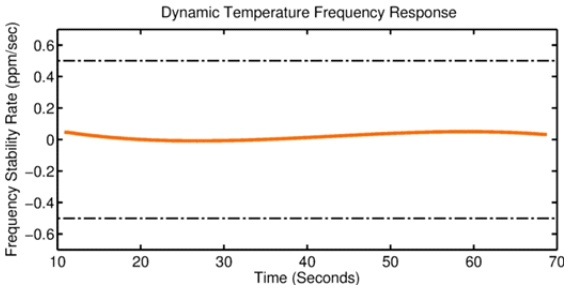


Dynamic Frequency Response for Moderate Temperature Ramps







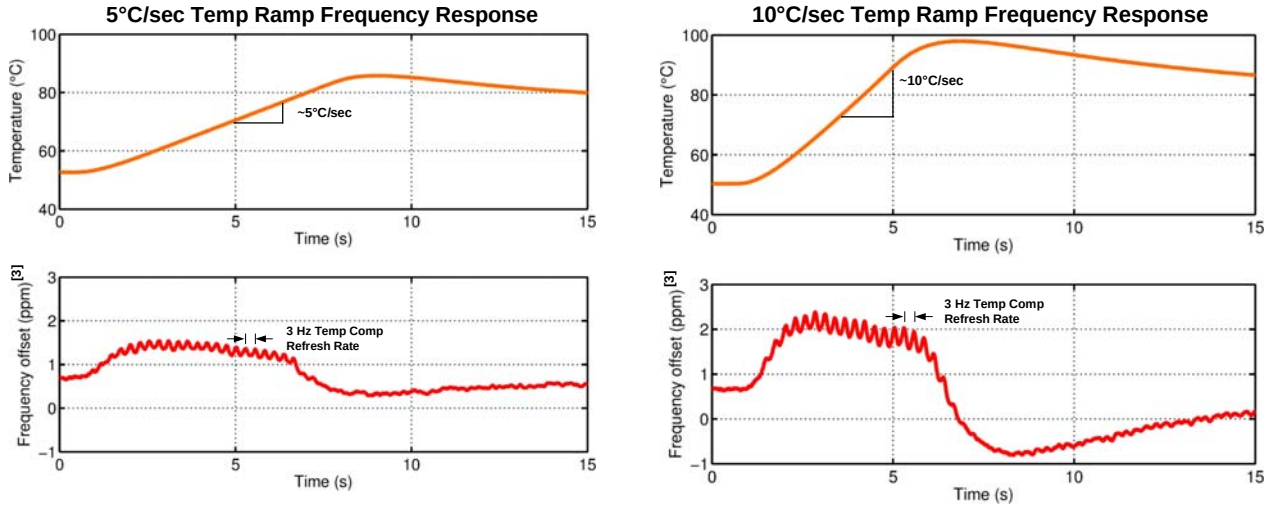


Frequency accuracy under a moderate temperature ramp up to 2°C/sec is limited by the TCXO's trimmed accuracy of the frequency stability over-temperature.

Note:

2. Measured relative to 32.768 kHz.

Dynamic Frequency Response for Fast Temperature Ramps



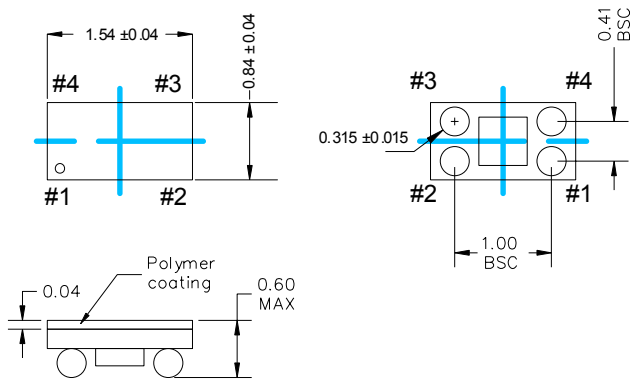
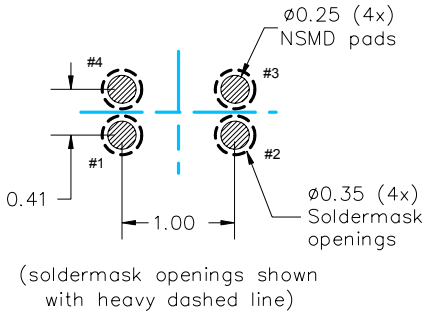
For temperature ramps >5°C/sec, the frequency accuracy is limited by the update rate of the temperature compensation path (see the 5°C/sec and 10°C/secplots).

Contact Factory for applications that require improved dynamic performance.

Note:

3. Measured relative to 32.768 kHz.

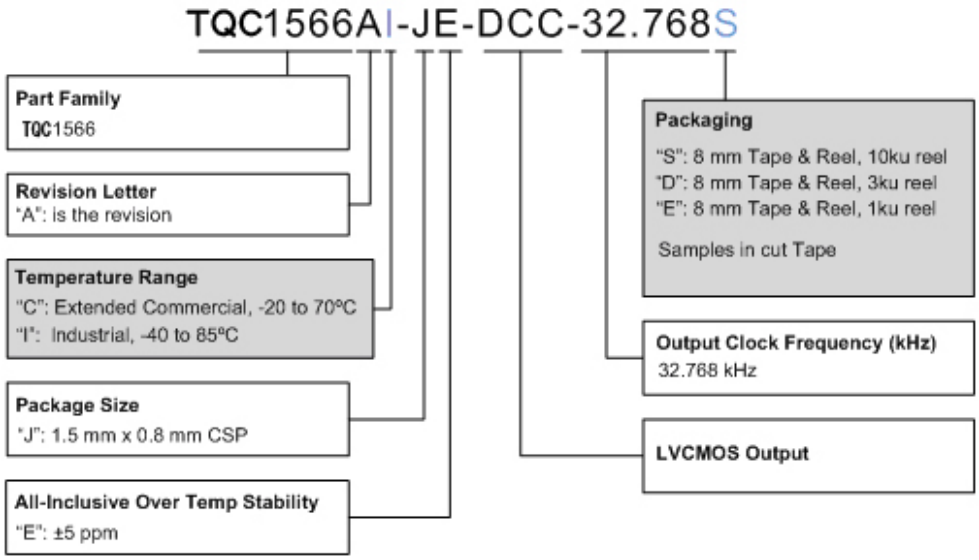
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
1.55 x 0.85 mm CSP 	 **Recommend 4-mil (0.1mm) stencil thickness**

Manufacturing Guidelines

1) No Ultrasonic or Megasonic cleaning: Do not subject TQC1566 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.
2) Applying board-level underfill and overmold is acceptable and will not impact the reliability of the device.
3) Reflow profile, per JESD22-A113D.
4) For additional manufacturing guidelines and marking/tape-reel instructions, click on the following link:

Ordering Information



Revision History

Revision	Release Date	Change Summary
0.1	6/30/15	Advanced datasheet initial release
0.7	3/11/16	Preliminary datasheet initial release